wherein the barrier metal is formed by using CVD of at least one of tungsten nitride WN_x, where x is an atomic fraction of N and comprises a range from 0.5 to 1.0, and tungsten silicide nitride WSi_yN_z, where y is an atomic fraction of Si and comprises a range from 0.01 to 0.2, and z is an atomic fraction of N and comprises a range from 0.02 to 0.2.

29. (New) The wiring structure according to claim 28, wherein an insulating layer, interposed between the first conducting layer and the second conducting layer to electrically isolate both conducting layers from each other, a hole is formed in the insulating layer so as to pass through the insulating layer, and the first conducting layer and the second conducting layer are electrically connected through the hole by way of the barrier metal.

30. (New) The wiring structure according to claim 29, wherein the barrier metal is interposed between the first conducting layer and the second conducting layer, or between the insulating layer and the first conducting layer and between the insulating layer and the second conducting layer.

31. (New) The wiring structure according to claim 29 or 30, wherein at least one of the first and second conducting layers is formed of Cu and the insulating layer is formed of any one of SiO_2, SiOF, and CF_x, where x is an atomic fraction of F from 1 to 4.

32. (New) The wiring structure according to claim 29, wherein the hole is a via-hole.

33. (New) The wiring structure according to claim 29, wherein one of the first conducting layer and the second conducting layer is formed of any one of Al, W, and Cu; and the other one of the first conducting layer and the second conducting layer is formed of any one of Co, W and Al.

34. (New) The wiring structure according to claim 29 wherein the hole is a contact hole.

35. (New) The wiring structure according to claim 34, wherein one of the first conducting layer and the second conducting layer is formed of any one of Al, W, and Cu; and the other one of the first conducting layer and the second conducting layer is formed of Si.

36. (New) An electrode of a circuit element formed on a semiconductor substrate, comprising

a polysilicon layer;

a barrier metal formed on the polysilicon layer; and

a metal layer formed on the barrier metal,

wherein the barrier metal is formed by using CVD of at least one of tungsten nitride WN_x, where x is an atomic fraction of N and comprises a range from 0.5 to 1.0, and tungsten silicide nitride WSi_yN_z, where y is an atomic fraction of Si and comprises a range from 0.01 to 0.2, and z is an atomic fraction of N and comprises a range from 0.02 to 0.2.

37. (New) The electrode according to claim 36, wherein the electrode is a gate electrode of a transistor; the polyisilicon layer is formed on a gate oxide film formed between a source and a drain of the transistor.

38. (New) The electrode according to claim 36 or 37, wherein the metal layer is formed any one of W, Cu and Al.

39. (New) The electrode according to claim 36, wherein the gate oxide film is formed of any one of SiO_2, SiOF, Ta_2O_5, and CF_x, where x is an atomic fraction of F from 1 to 4.

40. (New) A gate electrode of a translator formed on a semiconductor substrate, comprising:

a gate oxide film formed between a source and a drain of the transistor;

a barrier metal formed on the gate oxide film; and

a metal layer formed on the barrier metal,

wherein the barrier metal is formed by using CVD of at least one of tungsten nitride WN_x, where x is an atomic fraction of N and comprises a range from 0.5 to 1.0, and tungsten silicide nitride WSi_yN_z, where y is an atomic fraction of Si and comprises a range from 0.01 to 0.2, and z is an atomic fraction of N and comprises a range from 0.02 to 0.2.

41. (New) The electrode according to claim 40, wherein the metal layer is formed of any one of Al, W, and Cu.

42. (New) The electrode according to claim 40, wherein the gate oxide film is formed of any one of SiO_2, SiOF, Ta_2O_5, and CF_x, where x is an atomic fraction of F from 1 to 4.

43. (New) A method of forming a wiring structure of a semiconductor device, comprising:

forming a first conducting layer by depositing a metal film on an insulating film former on a semiconductor substrate;

forming an interlayer insulating film over an entire surface of the semiconductor substrate so as to cover the first conducting layer from the above;

forming a connecting hole at a predetermined position of the insulating film through the insulating film so as to expose the first conducting layer therein;

forming a barrier metal of at least one of tungsten nitride WN_x, where x is an atomic fraction of N and comprises a range from 0.5 to 1.0, and tungsten silicide nitride WSi_yN_z, where y is an atomic fraction of Si and comprises a range from 0.01 to 0.2, and z is an atomic fraction of N and comprises a range from 0.02 to 0.2 by using CVD on from an inner surface of the connecting hole to a surface of the first conducting layer exposed in a bottom portion of the connecting hole and an upper surface of the insulating film; and

depositing a metal film on the barrier metal layer and simultaneously filling the

connecting hole with the metal film, thereby foraging a second conducting layer electrically connected wish the first conducting layer via the barrier metal.

44. (New) The method according to claim 43, wherein the insulating film is an interlayer insulating film.

45. (New) The method according to claim 43, wherein at least one of the first and second conducting layers is formed of Cu and the interlayer insulating film is formed any one of SiO_2, SiOF, Ta_2O_5, and CF_x, where x is an atomic fraction of F from 1 to 4.

46. (New) The method according to claim 43, wherein the connecting hole is a via-hole.

47. (New) The method according to claim 43, wherein one of the first conducting layer and the second conducting layer is formed of any one of Al, W, and Cu, and the other one of the first conducting layer and the second conducting layer is formed of any one of W, Cu, and Al.

48. (New) A method of forming a wiring structure of a semiconductor device, comprising:

forming an insulating film on a semiconductor substrate having a first conducting layer;

forming a connecting hole at a predetermined position of the insulating film through the insulating film so as to expose the first conducting layer therein;

forming a barrier metal of at least one of tungsten nitride WN_x, where x is an atomic fraction of N and comprises a range from 0.5 to 1.0, and tungsten silicide nitride WSi_yN_z, where y is an atomic fraction of Si and comprises a range from 0.01 to 0.2, and z is an atomic fraction of N and comprises a range from 0.02 to 0.2 by using CVD from an inner surface of the connecting hole to a surface of the first conducting layer exposed in a bottom portion of

the connecting hole and to an upper surface of the insulating film; and

depositing a metal film on the barrier metal layer and simultaneously filling the connecting hole with the metal film, thereby forming a second conducting layer electrically connected with the first conducting layer via the barrier metal.

49. (New) The method according to claim 48, wherein the connecting hole is a contact hole.

50. (New) The method according to claim 48, wherein one of the first conducting layer and the second conducting layer is formed of any one of Al, W, and Cu and the other one of the first conducting layer and the second conducting layer is formed of Si.

51. (New) The method according to claim 48, wherein at least one of the first and second conducting layers is formed of Cu and the insulating film is formed any one of SiO_2, SiOF, Ta_2O_5, and CF_x, where x is an atomic fraction of F from 1 to 4.

52. (New) A method of forming a wiring structure of a semiconductor device, comprising:

forming an insulating film on a semiconductor substrate;

forming a wiring portion and a connecting hole simultaneously at a predetermined position of the insulating film through the insulating film so as to expose the first conducting layer;

forming a barrier metal layer of at least one of tungsten nitride WN_x, where x is an atomic fraction of N and comprises a range from 0.5 to 1.0, and tungsten silicide nitride WSi_yN_z, where y is an atomic fraction of Si and comprises a range from 0.01 to 0.2, and z is an atomic fraction of N and comprises a range from 0.02 to 0.2 by CVD from inner surfaces of the wiring portion and the connecting hole to a surface of the first conducting layer exposed in a bottom portion of the connecting hole and to an upper surface of the insulating

film;

depositing a metal film on the barrier metal layer and simultaneously filling the connecting hole with the metal film, thereby forming a second conducting layer electrically connected with the first conducting layer via the barrier metal; and

removing a residual metal film of the second conducting layer, thereby flattening the second conducting layer.

53. (New) The method according to claim 52, wherein a dual damascene structure is formed of the wiring portion and the connecting hole.

54. (New) The method according to claim 52, wherein one of the first conducting layer and the second conducting layer is formed of any one of Al, W, and Cu, and the other one of the first conducting layer and the second conducting layer is formed of any one of Si, Cu, W and Al.

55. (New) The method according to claim 52, wherein the insulating film is formed of any one of SiO_2, SiOF, Ta_2O_5, and CF_x, where x is an atomic fraction of F from 1 to 4.

56. (New) The method according to claim 52, wherein the metal film of the second conducting layer is flattened by CMP.

57. (New) A method of forming a gate electrode of a transistor formed on a semiconductor substrate, comprising:

forming a barrier metal layer of at least one of tungsten nitride WN_x, where x is an atomic fraction of N and comprises a range from 0.5 to 1.0, and tungsten silicide nitride WSi_yN_z, where y is an atomic fraction of Si and comprises a range from 0.01 to 0.2, and z is an atomic fraction of N and comprises a range from 0.02 to 0.2 by a thermal CVD method on a gate oxide film located between a drain and source of a transistor; and

forming a metal layer on the barrier metal layer.

58. (New) A method of forming a gate electrode of a transistor formed on a semiconductor substrate; comprising:

forming a polysilicon layer on a gate oxide film formed between a source and a drain of a transistor;

forming a barrier metal layer of at least one of tungsten nitride WN_x, where x is an atomic fraction of N and comprises a range from 0.5 to 1.0, and tungsten silicide nitride WSi_yN_z, where y is an atomic fraction of Si and comprises a range from 0.01 to 0.2, and z is an atomic fraction of N and comprises a range from 0.02 to 0.2 by a thermal CVD method; and

forming a metal film on the barrier metal layer.

59. (New) The method according to claims 57 or 58, wherein the metal layer comprises at least one of W and Cu.

60. (New) The method according to claims 57 or 58, wherein the gate oxide film comprises any one of SiO_2, SiOF, Ta_2O_5, and CF_x, where x is an atomic fraction of F from 1 to 4.

61. (New) The method according to claims 43, 48, 52, 57, and 58, wherein said WN has a W:N ratio of 1:0.5-1.0 and said WSiN has a W:Si:N ratio of 1 : 0.02-0.2 : 0.02-0.2.

62. (New) An electrode of a circuit element formed on a semiconductor substrate, comprising:

a polysilicon layer;

a barrier metal formed on the polysilicon layer; and

a metal layer formed on the barrier metal,

wherein the barrier metal comprises at least one of:

a tungsten layer and a tungsten nitride layer, and